Claims

What is claimed is:

1. A processor comprising:

scheduling circuitry for scheduling data blocks for transmission from a plurality of transmission elements; and

a priority computation element associated with the scheduling circuitry and operative to determine a transmission priority for one or more constituent transmission elements in a specified group of such transmission elements, the transmission priority being adjustable so as to facilitate the maintenance of a desired service level for one or more of the transmission elements.

2. The processor of claim 1 wherein the priority computation element operates under software control in at least one of determining and adjusting the transmission priority for the one or more constituent transmission elements.

3. The processor of claim 1 wherein the priority computation element comprises a script processor.

4. The processor of claim 1 wherein the group of transmission elements corresponds to a first level of an *n*-level hierarchy of transmission elements, the constituent transmission elements corresponding to at least one lower level of the *n*-level hierarchy of transmission elements.

5. The processor of claim 1 wherein each of the transmission elements comprises a queue.

6. The processor of claim 1 wherein the priority computation element determines an initial transmission priority for the constituent transmission elements of the group by designating a given one of the constituent transmission elements as a current high priority transmission element, with the other constituent transmission elements in the group being arranged in a linear order of decreasing priority relative to the current high priority transmission element.

7. The processor of claim 6 wherein the priority computation element subsequently adjusts the transmission priority for the constituent transmission elements of the group by designating another of the constituent transmission elements as the current high priority transmission element, with the remaining constituent transmission elements in the group being arranged in a linear order of decreasing priority relative to the current high priority transmission element.

8. The processor of claim 1 wherein the scheduling circuitry is configurable for utilization of at least one time slot table in scheduling the data blocks for transmission.

9. The processor of claim 1 wherein the priority computation element is operative to determine periodically if the transmission priority requires adjustment in order to maintain the desired service level for one or more of the transmission elements.

10. The processor of claim 9 wherein the priority computation element makes a determination as to whether the transmission priority requires adjustment, after transmission of a specified number of the data blocks.

11. The processor of claim 9 wherein the priority computation element makes the determination as to whether the transmission priority requires adjustment after transmission of each of the data blocks.

12. The processor of claim 1 further comprising traffic shaping circuitry coupled to the scheduling circuitry, the traffic shaping circuitry comprising the priority computation element.

13. The processor of claim 12 further comprising transmit queue circuitry coupled to the scheduling circuitry, wherein the transmission elements comprise one or more queues associated with the transmit queue circuitry, the transmit queue circuitry supplying time slot requests from the transmission elements to the scheduling circuitry in accordance with a traffic shaping requirement established by the traffic shaping circuitry.

14. The processor of claim 1 wherein one or more of the data blocks comprise data packets.

15. The processor of claim 1 wherein at least a subset of the constituent transmission elements have identifiers configured such that a given one of the transmission element identifiers can be linked to another of the transmission element identifiers so as to form a linked list of the corresponding transmission elements.

16. The processor of claim 1 wherein the processor comprises a network processor configured to provide an interface for data block transfer between a network and a switch fabric.

17. The processor of claim 1 wherein the processor is configured as an integrated circuit.

18. A method for use in a processor, the method comprising:

scheduling data blocks for transmission from a plurality of transmission elements;

wherein the scheduling step schedules the data blocks for transmission in accordance with a transmission priority determined for one or more constituent transmission elements in a specified group of such transmission elements, the transmission priority being adjustable so as to facilitate the maintenance of a desired service level for one or more of the transmission elements.

19. An article of manufacture comprising a machine-readable storage medium for use in conjunction with a processor, the medium storing one or more software programs for use in scheduling data blocks for transmission from a plurality of transmission elements, the one or more programs when executed providing at least one of determination of a priority for one or more constituent transmission elements in a specified group of such elements and adjustment of the transmission priority so as to facilitate the maintenance of a desired service level for one or more of the transmission elements.